NEX91X30-Q100

Automotive 300 mA, 40 V tracking LDO with 5 mV tolerance

Rev. 2.1 — 8 August 2025 Product data sheet

1. General description

The NEX91x30-Q100 is a Low-Dropout (LDO) voltage-tracking regulator with high tracking accuracy of 5 mV (max) and excellent load and line transient responses. It is specifically designed to power off-board sensors in automotive applications such as power train, safety, and Body Control Modules (BCMs). The device supports a wide input voltage range from 4 V to 40 V (up to 45 V transient) to withstand cold-crank and load-dump transient conditions.

The device output tracks the reference voltage applied to the EN/ADJ pin with an accuracy of ±5 mV over the specified temperature range for loads up to 300 mA. The high tracking accuracy ensures a precise power supply for off-board sensors and modules, improving the performance of radiometric sensors such as pressure and position sensors.

The device switches to standby mode by pulling down the EN/ADJ pin, which enables an ultra-low shutdown current of 0.75 µA typical to extend battery life. The device integrates protection features such as battery reverse polarity protection (-42 V), output reverse current protection, output short-to-battery and ground protection, current limit, and thermal shutdown. These protections guard against the high risk of cable failures in an off-board power system. The power-good (PG) output indicates an over voltage or under voltage condition of the tracking output.

The device operates across a temperature range from -40 °C to 125 °C ambient and -40 °C to 150 °C junction. It is available with thermal enhanced package SOT8063-2 (HSO8).

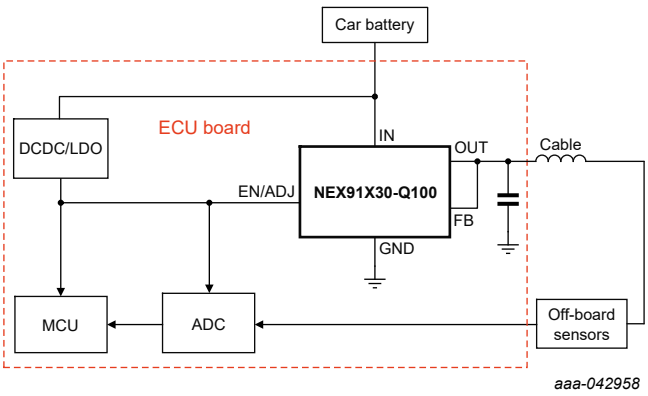


Fig. 1. Typical application

2. Features and benefits

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1 (T_{amb}): -40 °C to 125 °C
  - Junction temperature range (T_j): -40 °C to 150 °C
- Input voltage range: 4 V to 40 V
  - Absolute maximum input range: -42 V to 45 V
- Wide output voltage range: 2 V to 40 V
  - Absolute maximum output range: -5 V to 45 V
- Tight output tracking tolerance: ±5 mV
- Maximum output current: 300 mA
- Low dropout voltage: 440 mV typical at 300 mA (V_{OUT} = 5 V)
- Low quiescent current (I_Q):
  - 45 µA typical quiescent current at light loads
  - 0.75 µA typical shut-down current
- Over voltage and under voltage indication at PG output
- Active output discharge with a typical discharge current of 800 µA
- Stable with a wide range of ceramic output-stability cap: ESR from 0.001 Ω to 5 Ω; output capacitor from 4.7 µF to 470 µF
- Integrated various fault protections:
  - Reverse polarity protected input
  - Reverse current protection
  - Thermal shutdown
  - Short-circuit to ground and battery protection
  - Over-current protection
- HSO8 package available:
  - SOT8063-2 (HSO8): $R_{\theta JA}$ = 47.5 °C/W

3. Applications

- Supply for off-board sensors
- High precision voltage tracking
- Body Control Modules (BCMs)
- Power switch for off-board loads

Table 1. Device information

Part number	PG	Cable compensation
NEX91530PB-Q100	Y	N
NEX91630PB-Q100	N	Y
NEX91730PB-Q100	Y	Y (dynamic)

4. Ordering information

Table 2. Ordering information

Type number	Package			
	Temperature range (T_j)	Name	Description	Version
NEX91530PB-Q100	-40 °C to 150 °C	HSO8	Plastic, thermal enhanced small outline package; 8 leads; 1.27 mm pitch; 4.9 mm × 3.9 mm × 1.7 mm body	SOT8063-2
NEX91630PB-Q100				
NEX91730PB-Q100				

5. Marking

Table 3. Marking codes

Type number	Marking code
NEX91530PB-Q100	N91530
NEX91630PB-Q100	N91630
NEX91730PB-Q100	N91730

6. Pin configuration and description

6.1. Pin configuration

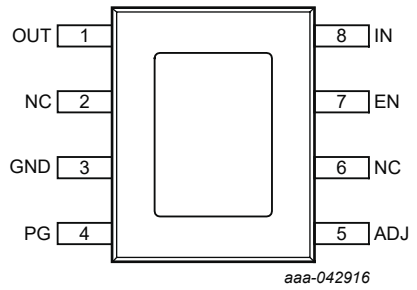


Fig. 2. NEX91530PB-Q100

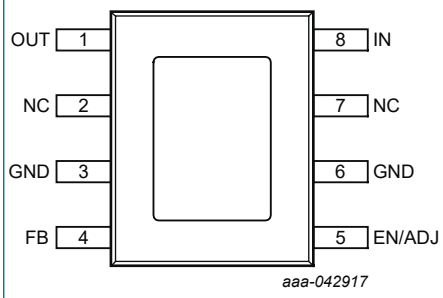


Fig. 3. NEX91630PB-Q100

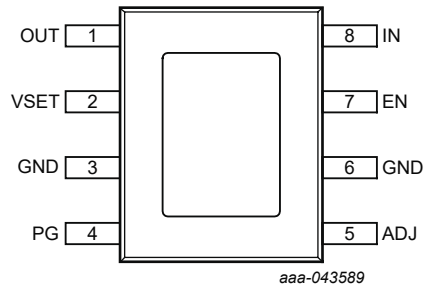


Fig. 4. NEX91730PB-Q100

6.2. Pin description

Symbol			Pin	I/O	Description
NEX91530-Q100	NEX91630-Q100	NEX91730-Q100			
OUT	OUT	OUT	1	O	**OUT**: tracking output voltage pin. Place a capacitor as close to the output of the device as possible, follow the capacitance and ESR requirements described in Table 7.
NC	NC	VSET	2	I	**NC**: not connected pin. It is not connected internally and can be tied to the ground plane to enhance thermal dissipation. **VSET**: cable compensation pin.
GND	GND	GND	3	G	**GND**: ground pin. This pin is connected to ground internally.
PG	FB	PG	4	O	**PG**: power-good pin. It is an open-drain pin that must connect to positive voltage rail via an external pull-up resistor. V_{PG} is logic level high when V_{OUT} is above or lower the power-good threshold. If not used, can be left floating. **FB**: feedback pin. External resistor used to set the max cable comp voltage at full load current, there is no cable comp voltage when pull to out pin.
ADJ	EN/ADJ	IN	5	I	**ADJ**: adjustable voltage pin, can be connected directly to the reference voltage or through a resistor divider for lower voltage. Place a capacitor close to the ADJ pin to eliminate line interference. For enable function, a low voltage signal disables the device, while a high voltage signal enables it. **EN/ADJ**: enable and adjustable voltage pin. **IN**: input power-supply voltage pin. Place a small ceramic capacitor as close to the input of the device as possible to reduce line interference.
NC	GND	EN	6	G	**NC**: not connected pin. It is not connected internally and can be tied to the ground plane to enhance thermal dissipation. **GND**: ground pin. This pin is connected to ground internally. **EN**: enable pin. A low voltage signal disables the device, while a high voltage signal enables it.

Symbol			Pin	I/O	Description
NEX91530 -Q100	NEX91630 -Q100	NEX91730 -Q100			
EN	NC	GND	7	I	**EN**: enable pin. A low voltage signal disables the device, while a high voltage signal enables it. **NC**: not connected pin. It is not connected internally and can be tied to the ground plane to enhance thermal dissipation. **GND**: ground pin. This pin is connected to ground internally.
IN	IN	ADJ	8	I	**IN**: input power-supply voltage pin. Place a small ceramic capacitor as close to the input of the device as possible to reduce line interference. **ADJ**: adjustable voltage pin, can be connected directly to the reference voltage or through a resistor divider for lower voltage. Place a capacitor close to the ADJ pin to eliminate line interference. For enable function, a low voltage signal disables the device, while a high voltage signal enables it.
Exposed thermal pad				-	Not connected internally. It can be left floating, but for better thermal performance it is recommended to connect it to the GND.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	unregulated input voltage		-42	45	V
V_{OUT}	tracking output voltage		-5	45	V
V_{EN}	enable output voltage		-42	45	V
V_{ADJ}	adjustable voltage		-42	45	V
V_{FB}	feedback voltage		-5	45	V
V_{PG}	power-good voltage		-0.3	6.6	V
V_{VSET}	VSET voltage		-0.3	6.6	V
T_j	operating junction temperature		-40	150	°C
T_{amb}	operating ambient temperature		-40	125	°C
T_{stg}	storage temperature		-65	165	°C

[1] Stresses beyond those conditions under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8. ESD ratings

Table 5. ESD ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 3A [1]	-4000	-	4000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C3 [2]	-1000	-	1000	V

[1] HBM stress testing was performed in accordance with AEC-Q100-002.
[2] CDM stress testing was performed in accordance with AEC-Q100-011.

9. Thermal Information

Table 6. Thermal information

Thermal resistance according to JEDEC51-5 and -7.

Symbol	Parameter	SOT8063-2 (HSO8)	Unit
$R_{\theta JA}$	junction to ambient thermal resistance	47.5	°C/W
$R_{\theta JC(top)}$	junction to case (top) thermal resistance	78.8	°C/W
$R_{\theta JB}$	junction to board thermal resistance	22.8	°C/W
Ψ_{JT}	junction to top char parameter	9.5	°C/W

10. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	input voltage		4	-	40	V
V_{OUT}	output voltage		2	-	40	V
I_{OUT}	output current	[1]	-	-	300	mA
V_{ADJ}	adjust input voltage range (voltage tracking range)		2	-	40	V
V_{EN}	enable voltage		0	-	40	V
C_{IN}	input capacitance		0.47	1	-	µF
C_{OUT}	output capacitance	[2]	4.7	-	470	µF
ESR	output capacitor ESR requirements	[3]	0.001	-	5	Ω
T_{amb}	ambient temperature		-40	-	125	°C
T_j	junction temperature		-40	-	150	°C

[1] Maximum output current when device is not thermal shutdown.
[2] The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.
[3] Relevant ESR value at f = 10 kHz, if using a large ESR capacitor it is recommended to decouple this with a 100 nF ceramic capacitor to improve transient performance.

11. Electrical characteristics

Table 8. Electrical characteristics

At recommended operating conditions; T_j = -40 °C to 150 °C; C_{OUT} = 4.7 µF; V_{IN} = 13.5 V; I_{OUT} = 100 µA; V_{ADJ} = 5 V; (unless otherwise noted) voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		T_{amb} = -40 °C to 125 °C			Unit
				Min	Typ[1]	Max	
Power supply							
V_{IN}	input voltage range			4	-	40	V
$V_{IN(UVLO)}$	under voltage lockout threshold	V_{IN} rising		-	3.6	3.9	V
		V_{IN} falling		-	3.2	3.5	V
		hysteresis		-	400	-	mV
I_Q	quiescent current	V_{IN} = 5.5 V to 40 V; I_{OUT} = 100 µA; V_{ADJ} = 5 V	NEX91630PB-Q100	-	45	70	µA
			NEX91530PB-Q100	-	85	110	µA
			NEX91730PB-Q100	-	85	120	µA

Symbol	Parameter	Conditions		T_{amb} = -40 °C to 125 °C			Unit
				Min	Typ[1]	Max	
I_{GND}	ground current	V_{IN} = 13.5 V; I_{OUT} ≤ 300 mA; V_{ADJ} = 5 V [2]		-	400	-	µA
I_{STD}	stand-by current	V_{IN} = 4 V to 40 V; V_{EN} ≥ 2 V; V_{ADJ} < 0.7 V		-	6.4	15	µA
I_{SHUT}	shutdown current	V_{IN} = 4 V to 40 V; V_{EN} = 0 V		-	0.75	3.5	µA
$I_{R(IN)}$	reverse current at IN	V_{IN} = 0 V; V_{OUT} = 40 V; V_{ADJ} = 5 V		-5	-	0	µA
$I_{R(-IN)}$	reverse current at negative IN	V_{IN} = -40 V; V_{OUT} = 0 V; V_{ADJ} = 5 V		-10	-	0	µA
EN/ADJ and FB pin							
V_{EN_L}	logic input low level			-	-	0.7	V
V_{EN_H}	logic input high level			2	-	-	V
I_{EN}	EN pin current	V_{IN} = 13.5 V; V_{EN} = 5 V		-	-	100	nA
V_{ADJ_H}	adjust high signal valid	$\|V_{OUT} - V_{ADJ}\|$ ≤ 5 mV		1.8	-	-	V
V_{ADJ_L}	adjust low signal valid	V_{OUT} = 0 V		-	-	0.7	V
I_{ADJ}	adjust input current	V_{IN} = 13.5 V; V_{EN} = V_{ADJ} = 5 V	NEX91530PB-Q100	-	-	600	nA
			NEX91730PB-Q100	-	-	600	nA
			NEX91630PB-Q100	-	-	800	nA
I_{FB}	FB pin current	V_{ADJ} = V_{FB} = 5 V		-	-	5	µA
Output							
V_{OUT}	output accuracy	V_{IN} = 1 V + V_{OUT} to 40 V (V_{IN} ≥ 4 V; I_{OUT} = 100 µA to 300 mA		-5	-	5	mV
$\Delta V_{OUT(\Delta VIN)}$	line regulation	V_{IN} = 5.5 V to 40 V; I_{OUT} = 10 mA; V_{ADJ} = 5 V		-	-	0.5	mV
$\Delta V_{OUT(\Delta IOUT)}$	load regulation	V_{IN} = 6 V to 40 V; I_{OUT} = 100 µA to 300 mA; V_{ADJ} = 5 V		-	-	2	mV
V_{DO}	dropout voltage	V_{DO} = V_{IN} - V_{OUT}; V_{IN} = V_{ADJ} = 5 V	I_{OUT} = 200 mA	-	290	470	mV
			I_{OUT} = 300 mA	-	440	690	
I_{OUT}	output current	V_{IN} = V_{ADJ} + 1 V		-	-	300	mA
I_{DIS}	discharge current	V_{OUT} = 5 V; V_{IN} = 13.5 V		-	800	-	µA
I_{CL}	output current limit	V_{IN} = 13.5 V; output short to 90% x V_{ADJ}		310	420	600	mA
PSRR	power-supply ripple rejection	V_{IN} = 13.5 V; V_{ADJ} = 5 V; I_{OUT} = 10 mA; C_{OUT} = 4.7 µF; frequency = 100 Hz [2]		-	85	-	dB
V_n	output noise voltage	V_{ADJ} = 5 V; I_{OUT} = 1 mA; BW = 10 Hz to 100 kHz; 5 µVRMS reference [3]		-	50	-	µVRMS
Power-good							
$V_{PG\ (UV)}$	power-good switching threshold; under-voltage	V_{OUT} decreasing; power-good from high to low; V_{OUT} - V_{ADJ}		-220	-130	-50	mV
$V_{PG\ (OV)}$	power-good switching threshold; over-voltage	V_{OUT} increasing; power-good from high to low; V_{OUT} - V_{ADJ}		50	130	220	mV
t_{PG_R}	power-good reaction time			-	15	40	µs
t_{PG_D}	power-good deglitch time			-	250	470	µs
V_{PG_L}	PG pin low level output voltage	sink 1 mA current		-	0.2	0.4	V
I_{PG}	power-good output leakage current	V_{IN} = 13.5 V; V_{PG} = 5 V		-	-	100	nA

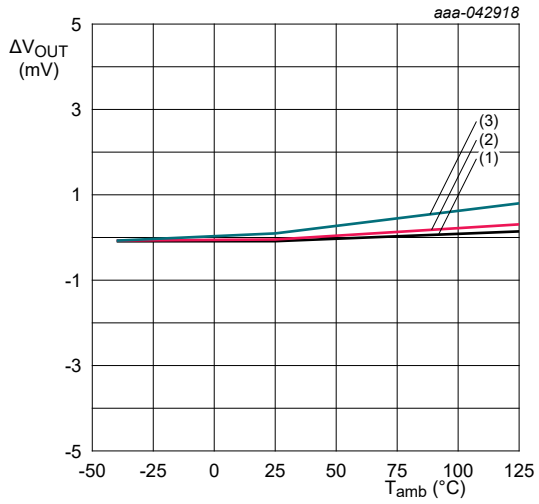
Symbol	Parameter	Conditions	T_{amb} = -40 °C to 125 °C			Unit
			Min	Typ[1]	Max	
Cable compensation (NEX91730PB-Q100)						
V_{OUT} - V_{ADJ}	cable compensation voltage	V_{SET} = GND	-5	0	5	mV
		V_{SET} = 75 kΩ; V_{ADJ} = 5 V; I_{OUT} = 100 mA	70	95	110	mV
		V_{SET} = 75 kΩ; V_{ADJ} = 5 V; I_{OUT} = 300 mA	250	285	320	mV
I_{VSET}	VSET pin current	V_{IN} = 13.5 V; V_{SET} = 5 V	-	-	100	nA
Operating temperature range						
T_{SD}	junction thermal shutdown temperature	rising junction temperature [2]	-	175	-	°C
T_{HYST}	thermal shutdown hysteresis	[2]	-	20	-	°C

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Guaranteed by bench test, not fully tested in production.
[3] Guaranteed by design.

12. Typical characteristics

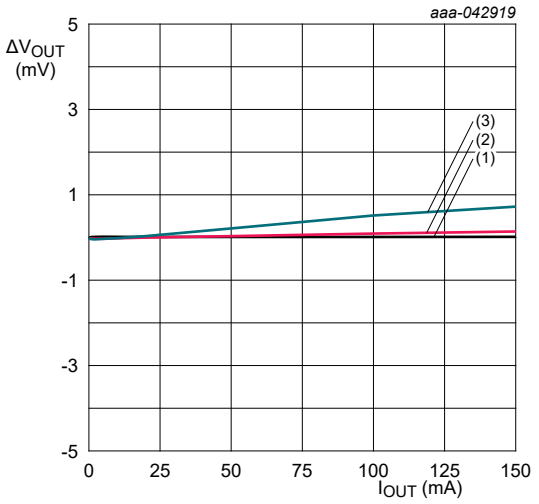
At recommended operating conditions, voltages are referenced to GND (ground = 0 V), and typical values are at 25 °C (unless otherwise noted).

V_{IN} = 13.5 V; V_{ADJ} = 5 V; C_{IN} = 1 µF; C_{OUT} = 4.7 µF; unless otherwise specified.



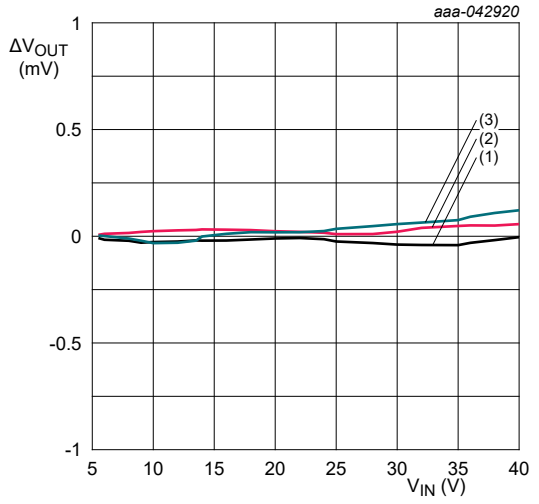
V_{IN} = 13.5 V; V_{ADJ} = 5 V; $\Delta V_{OUT} = V_{ADJ} - V_{OUT}$
(1) I_{OUT} = 100 µA
(2) I_{OUT} = 50 mA
(3) I_{OUT} = 150 mA

Fig. 5. Tracking accuracy vs ambient temperature



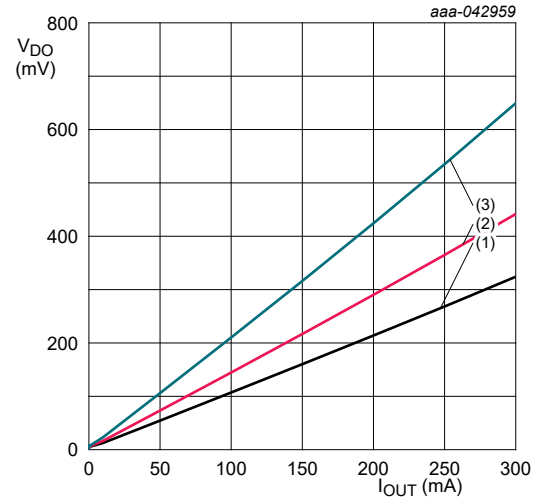
V_{IN} = 13.5 V; V_{ADJ} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 6. Load regulation



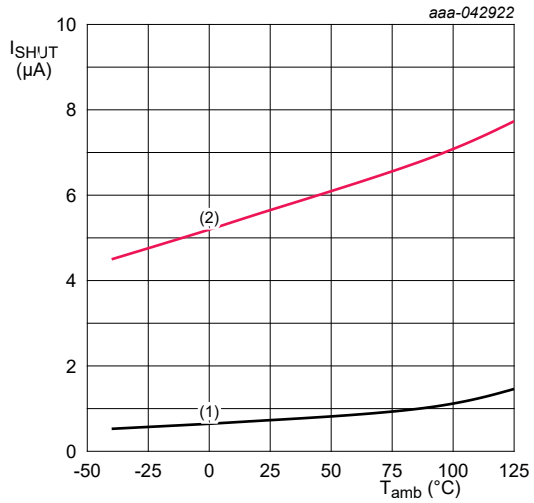
V_{ADJ} = 5 V; I_{OUT} = 10 mA
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 7. Line regulation



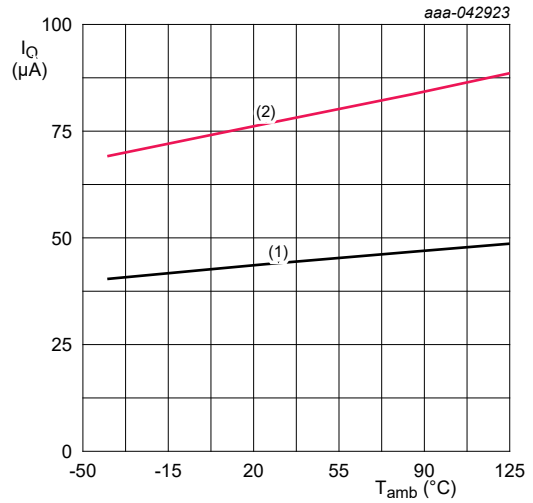
V_{ADJ} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 8. Dropout voltage vs output current



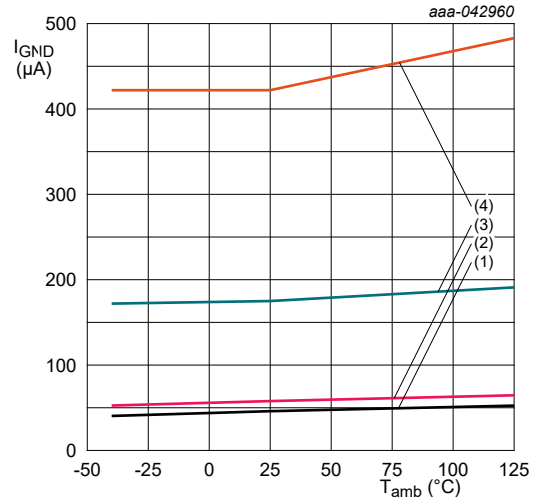
$V_{EN/ADJ}$ < 0.7 V
(1) $V_{EN/ADJ}$ < 0.7 V
(2) V_{ADJ} < 0.7 V; V_{EN} ≥ 2 V

Fig. 9. Shutdown current vs ambient temperature



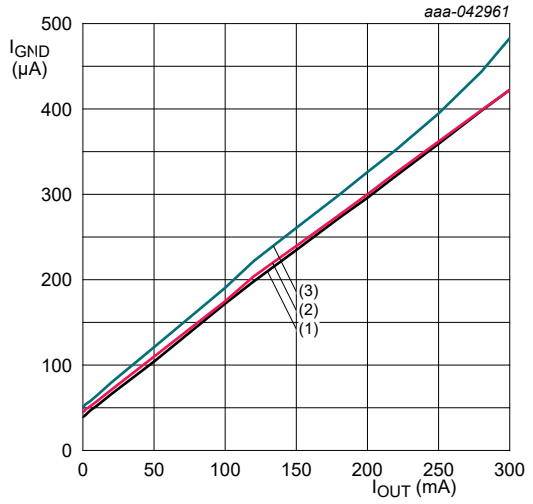
I_{OUT} = 100 µA
(1) NEX91630PB-Q100
(2) NEX91530PB-Q100/NEX91730PB-Q100

Fig. 10. Quiescent current vs ambient temperature



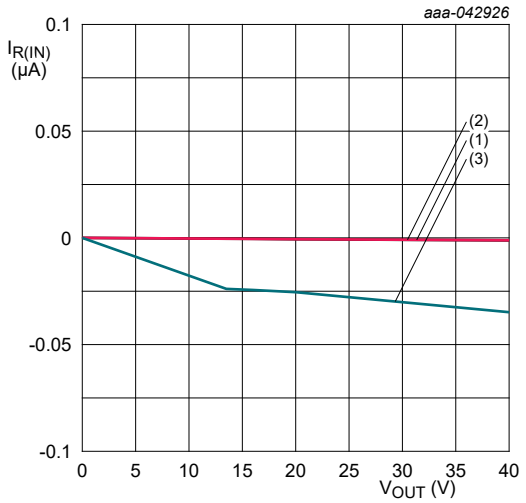
V_{IN} = 9 V; V_{ADJ} = 5 V
(1) I_{OUT} = 1 mA
(2) I_{OUT} = 10 mA
(3) I_{OUT} = 100 mA
(4) I_{OUT} = 300 mA

Fig. 11. Ground current vs ambient temperature



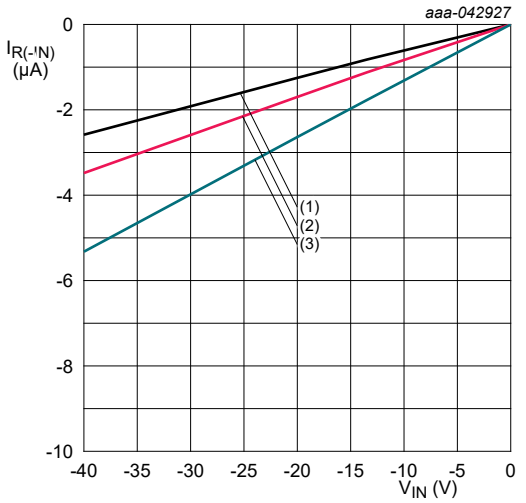
V_{IN} = 9 V; V_{ADJ} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 12. Ground current vs output current



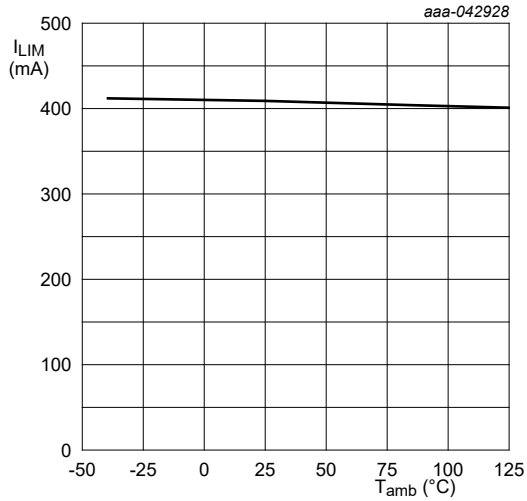
V_{ADJ} = 5 V; V_{IN} = 0 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 13. Reverse current vs output voltage



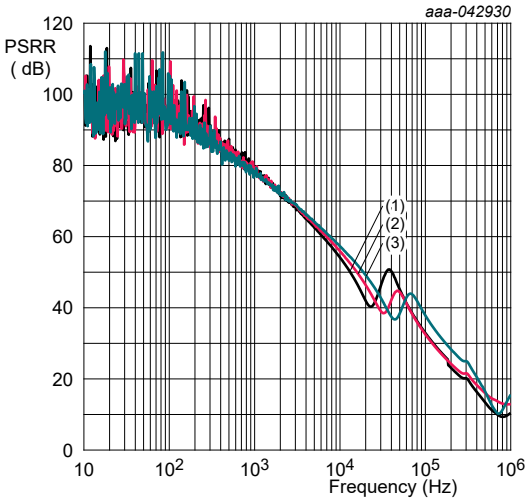
V_{ADJ} = 5 V; V_{OUT} = 0 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 125 °C

Fig. 14. Reverse current vs input voltage



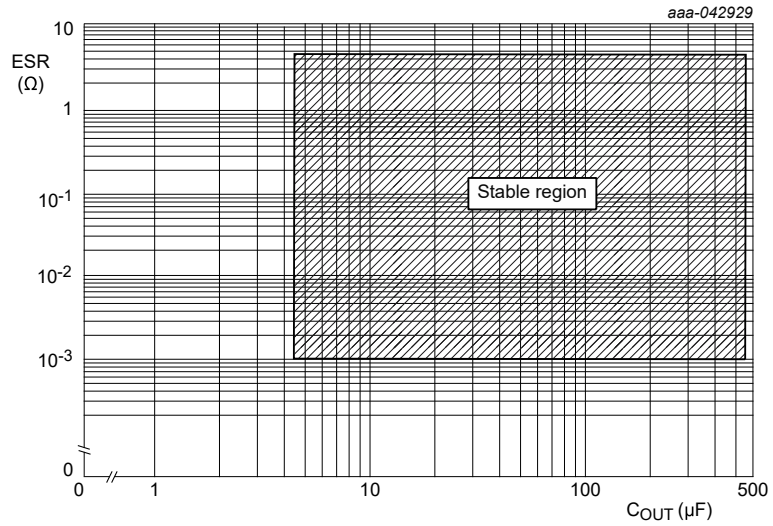
V_{IN} = 13.5 V; V_{ADJ} = 5 V

Fig. 15. Current limit vs temperature



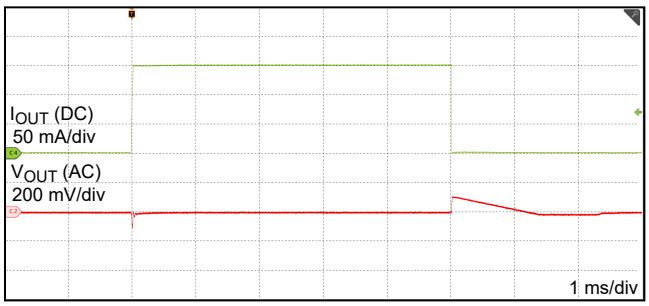
V_{IN} = 13.5 V; V_{ADJ} = 5 V;
C_{IN} = 0.1 µF; C_{OUT} = 4.7 µF
(1) I_{OUT} = 10 mA
(2) I_{OUT} = 50 mA
(3) I_{OUT} = 150 mA

Fig. 16. PSRR



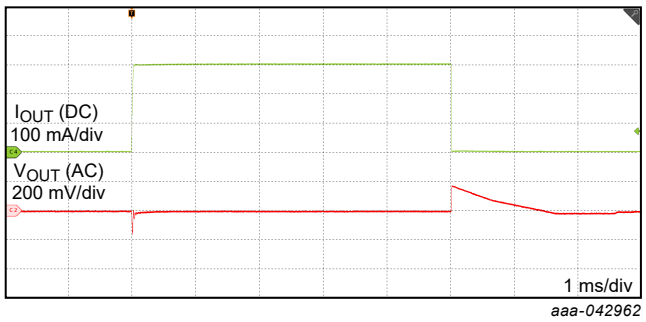
1 mΩ ≤ ESR ≤ 5 Ω; 4.7 µF ≤ C_{OUT} ≤ 470 µF

Fig. 17. ESR vs load capacitance



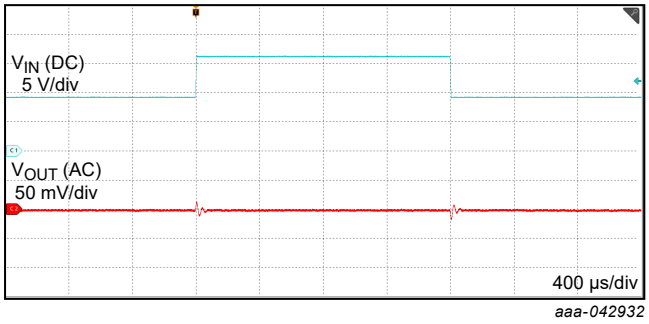
V_{IN} = 13.5 V; I_{OUT} = 0 mA to 150 mA;
slew rate = 1 A/µs; V_{ADJ} = 5 V; C_{OUT} = 10 µF

Fig. 18. Load transient



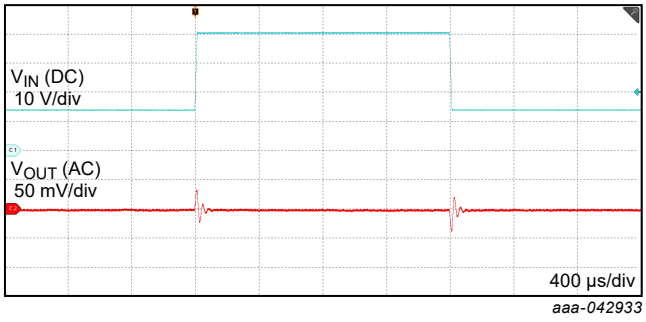
V_{IN} = 13.5 V; I_{OUT} = 0 mA to 300 mA;
slew rate = 1 A/µs; V_{ADJ} = 5 V; C_{OUT} = 10 µF

Fig. 19. Load transient



V_{IN} = 9 V to 16 V; slew rate = 1 V/µs;
V_{ADJ} = 5 V; I_{OUT} = 150 mA; C_{OUT} = 10 µF

Fig. 20. Line transient



V_{IN} = 13.5 V to 40 V; slew rate = 1 V/µs;
V_{ADJ} = 5 V; I_{OUT} = 150 mA; C_{OUT} = 10 µF

Fig. 21. Line transient

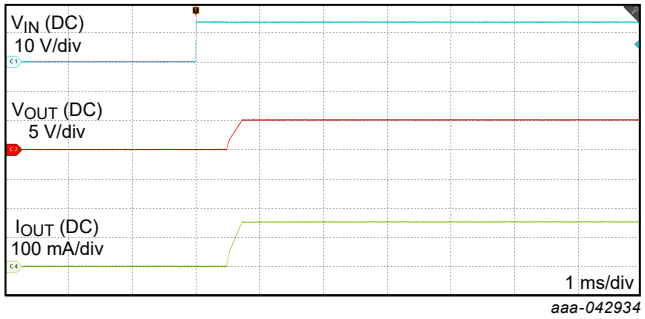


Fig. 22. Start up by VIN

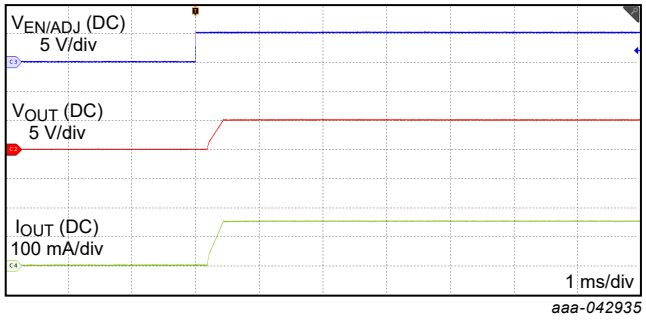


Fig. 23. Start up by EN/ADJ

13. Detailed description

13.1. Overview

The NEX91x30-Q100 is a Low-Dropout (LDO) tracking regulator with ultra-low tracking tolerance and out. It is designed to supply off-board systems, such as sensors in power train or passive safety applications. The device offers multiple protection features, including reverse polarity protection and safeguards against shorts to the battery and ground. In addition, this device also features thermal shutdown protection in case of an over temperature event.

13.2. Function block diagrams

Fig. 24 shows the function block diagram of NEX91530-Q100 and NEX91630-Q100, and Fig. 25 shows the function block diagram of NEX91730-Q100.

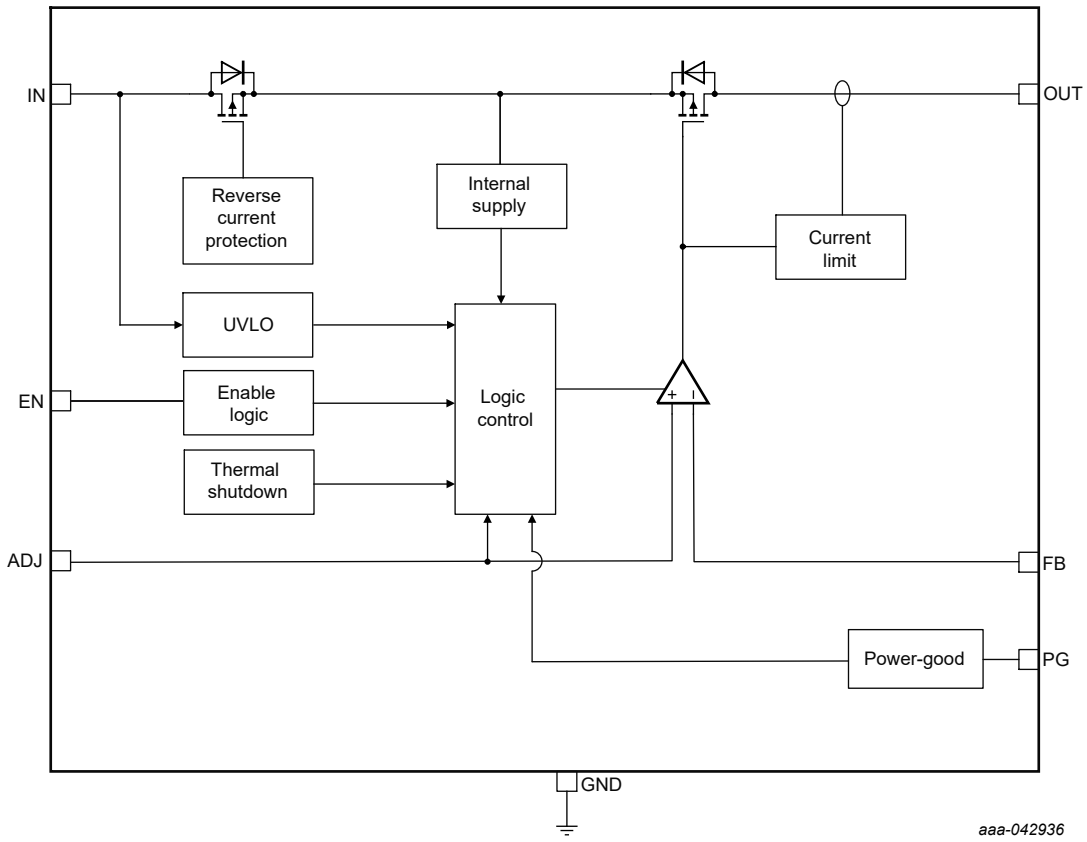


Fig. 24. Function block diagram of NEX91530-Q100 and NEX91630-Q100

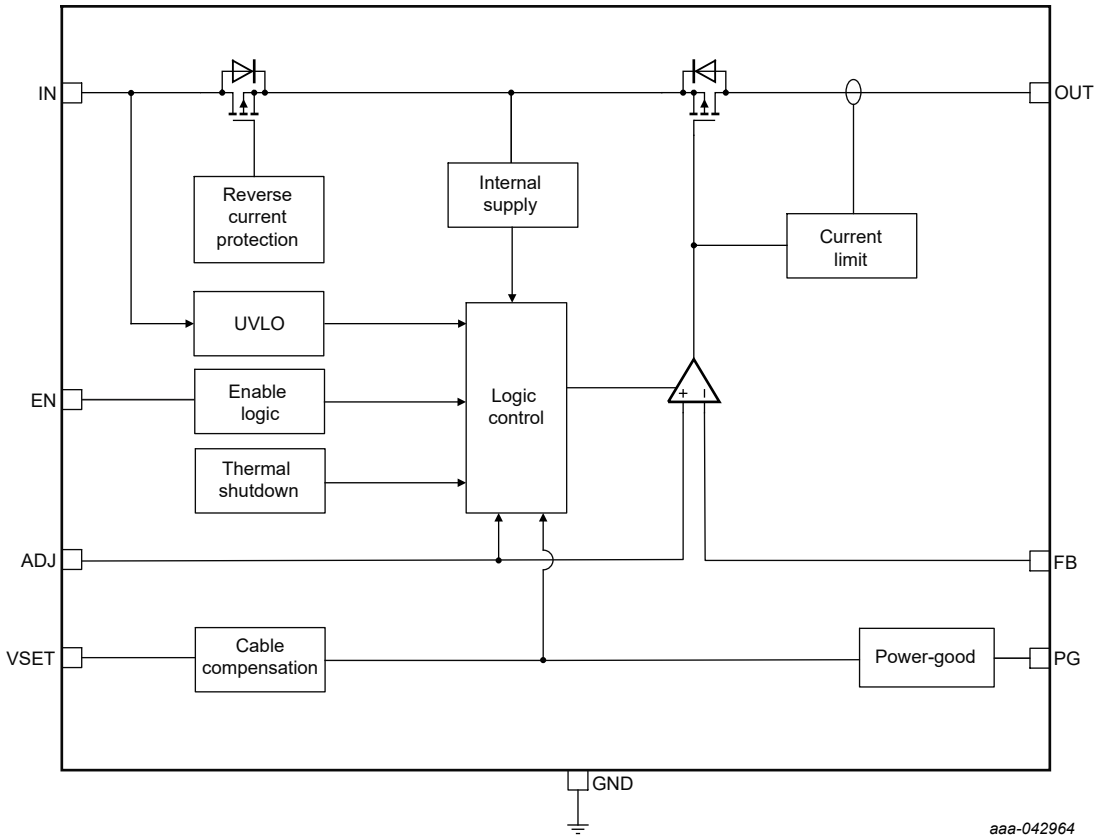


Fig. 25. Function block diagram of NEX91730-Q100

13.3. Feature description

13.3.1. Tracking output (V_{OUT})

The output voltage precisely follows the reference voltage applied to the ADJ input. This supports output voltage up to 40 V and current up to 150 mA. When the ADJ pin voltage exceeds the enable threshold voltage, the output begins rising to match the ADJ voltage. The output then increases linearly based on three factors: load conditions, output capacitance, and current limit. Once the output voltage reaches the ADJ pin voltage level, it stops rising and remains stable within ±5 mV of the reference voltage.

13.3.1.1. Output voltage equal to reference voltage

As shown in Fig. 26, the output voltage of the LDO output voltage is equal to the reference voltage within a tolerance of ±5 mV. This is achieved by directly applying an external reference voltage to the reference pin, while the FB pin (NEX91630-Q100 only) is connected to OUT pin. The output voltage can be expressed as: $V_{OUT} = V_{REF}$.

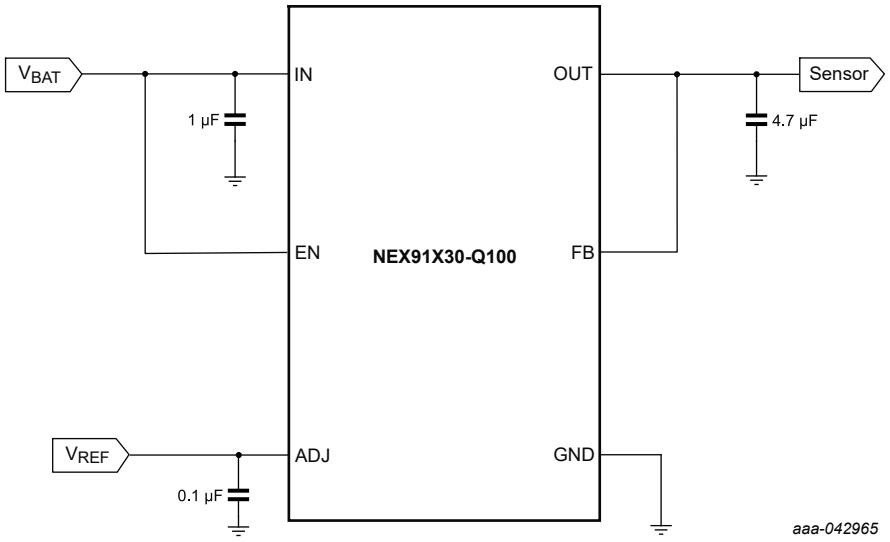


Fig. 26. Output voltage equal to reference voltage

13.3.1.2. Output voltage less than the reference voltage

As shown in Fig. 27, the LDO output voltage can achieve lower output voltage than the reference voltage. The output voltage can be expressed as: $V_{OUT} = \frac{V_{REF} \times R2}{R1 + R2}$

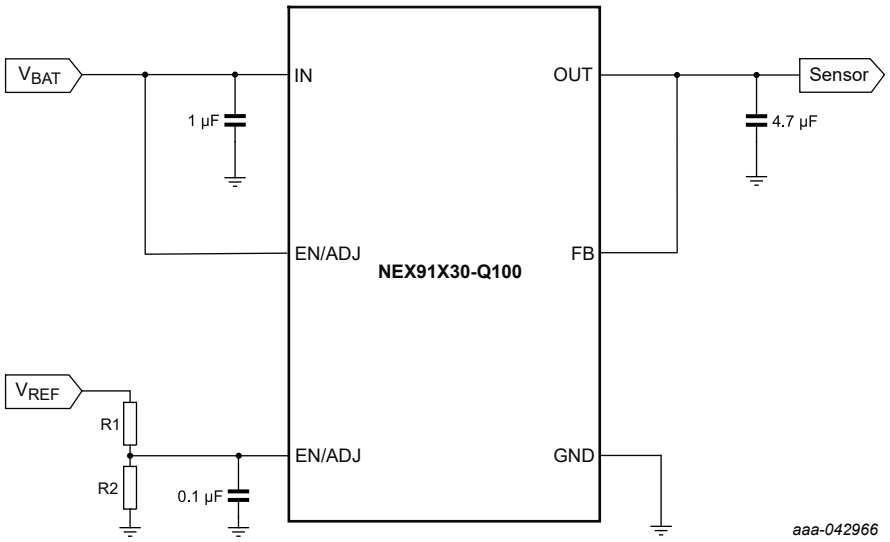


Fig. 27. Output voltage less than reference voltage

13.3.1.3. Output voltage larger than the reference voltage

In practical applications, the output of the tracker is used to supply power to the off-board load through a cable. The equivalent resistance of the cable gives rise to a voltage drop, which may result in an inadequate power supply for the off-board load. This problem can be mitigated by implementing cable compensation strategies to counteract the voltage drop occurring within the cable. Generally, two main approaches are available: fixed cable compensation and dynamic cable compensation.

13.3.1.3.1. Fixed cable compensation

An external resistive divider connected between the OUT and FB pins can be configured to generate an output voltage exceeding the reference voltage (ADJ), as illustrated in the Fig. 28. The output voltage is defined by:

$$V_{OUT} = \frac{V_{REF} \times (R1 + R2)}{R2}$$

R1 and R2 should ideally be in the range of 10 kΩ to 100 kΩ.

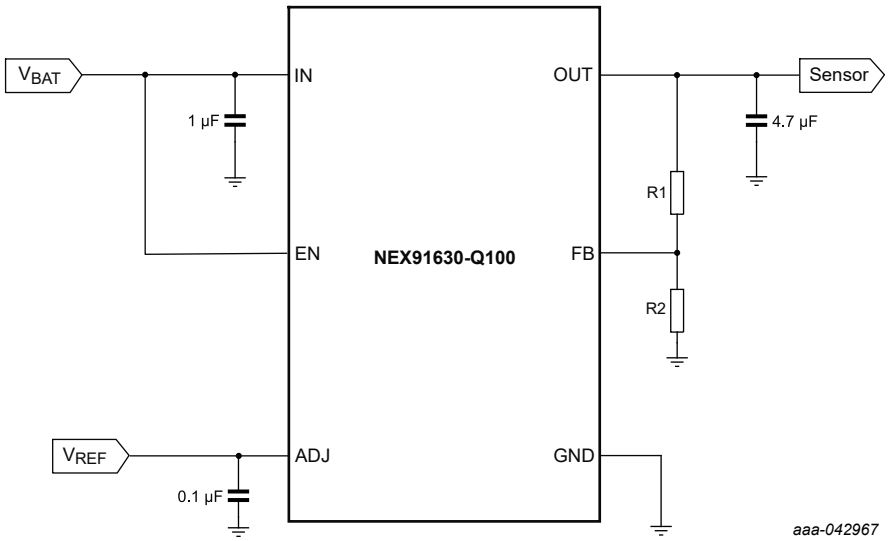


Fig. 28. Output voltage larger than reference voltage

13.3.1.3.2. Adjustable cable compensation

NEX91730-Q100 implements dynamic cable loss compensation by adjusting the resistance value at the VSET pin as shown in Fig. 29. This feature enables the device to automatically regulate the output voltage according to real-time load conditions and cable impedance, ensuring enhanced system accuracy. The compensation resistance R_{SET} is calculated as:

$$R_{SET} = \frac{\Delta V_{OUT}}{N}$$

$\Delta V_{OUT} = R_{total} \times I_{OUT}$, R_{total} includes the resistance of all traces, including the cables and PCB trace.The value of N is determined by internal circuit design, with a typical value of $N = 4 \times 10^{-6}$. Refer to the detailed range in Table 8 (V_{OUT} - V_{ADJ}) to set the maximum compensation voltage. C_{COMP} is used for LDO loop stability and $C_{COMP} \geq C_{OUT} / 3000$.

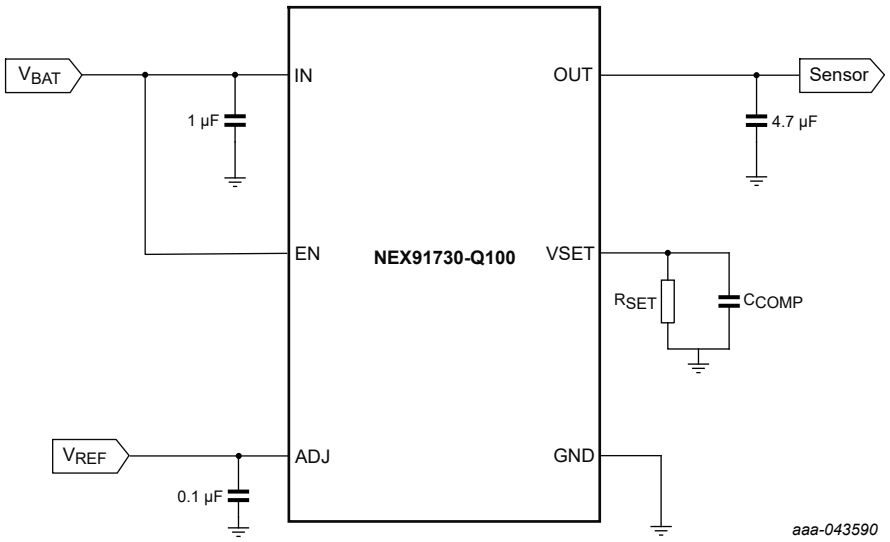


Fig. 29. Output voltage larger than reference voltage

The typical resistance value as shown in Table 9 based on different compensation voltage.

Table 9. Cable compensation voltage setting (maximum compensation voltage)

ΔV_{OUT} at 300 mA full load (mV)	R_{SET} (kΩ)
320	75
110	24.9

13.3.2. Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit is to stop the operation of the device when the input voltage falls below the typical threshold $V_{IN(UVLO)}$. The UVLO circuit includes hysteresis to prevent the device from shutting down if input voltage drops briefly after power up, as specified in the Electrical Characteristics table. If the input voltage experiences a negative transient that drops below the UVLO threshold and then recovers, the regulator will shut down and restart following the normal power-up sequence once the input voltage exceeds the required level.

13.3.3. Current limit operation

The device features an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. When the device is in current limit mode, the output voltage is not regulated. During a current limit event, the device heats up due to increased power dissipation. When the device reaches the current limit (I_{CL}), the pass transistor dissipates power according to the formula [(V_{IN} – V_{OUT}) x I_{CL}]. If thermal shutdown is triggered, the device will turn off. Once it cools down, the internal thermal shutdown circuit will turn the device back on. If the output current fault condition persists, the device will cycle between current limit and thermal shutdown.

13.3.4. Thermal protection

The NEX91x30-Q100 integrates an internal temperature sensor to monitor the junction temperature (T_j). If the T_j exceeds the thermal shutdown temperature (T_{SD}) of 175 °C, the device ceases operation. The device will resume functioning when T_j drops below the hysteresis threshold of approximately 20 °C.

Thermal shutdown may be triggered during start-up due to large inrush currents charging substantial output capacitance, or under heavy loads where high (V_{IN} – V_{OUT}) regulations result in significant power dissipation across the die. Proper heat sinking should be considered in these high-power dissipation scenarios.

13.3.5. Output short to battery and reverse protection

The NEX91x30-Q100 employs a back-to-back PMOS topology to protect the device from damage during fault conditions where V_{OUT} exceeds V_{IN}, effectively blocking reverse current flow. The device remains undamaged as long as it operates within the parameters provided in Limiting values. This integrated protection eliminates the requirement for an external diode.

The NEX91x30-Q100 remains undamaged, even when the output is shorted to the battery (see Fig. 30, with NEX91630-Q100 as the example). A short to the battery might occur when the device is powered by a lower separated input voltage supply as shown in Fig. 31. In this example, the input supply is set to 9 V. When a short to the battery (13.5 V typical) occurs on output that typically runs at 5 V, the continuous reverse current that flows out through the input is less than 5 µA.

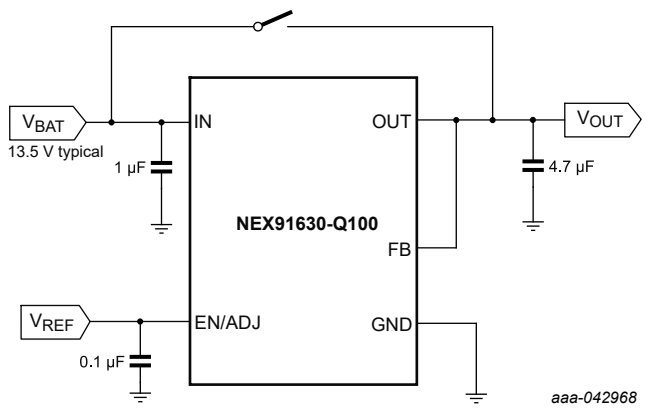


Fig. 30. Output short to battery

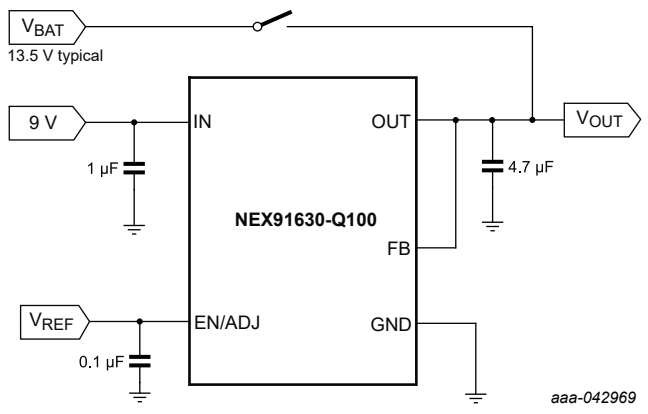


Fig. 31. Output short to battery with lower input voltage

13.3.6. Active output discharge

The device incorporates an active output discharge function when enabled, ensuring the output voltage rapidly returns to its nominal level during over-voltage fluctuations. This is particularly effective during load transients such as heavy-to-light load transitions. When the output voltage exceeds the nominal level, the device activates a FET that connects a resistor with a resistance value of several thousand ohms in series with the ground to achieve active discharge. Under these conditions, the output sources a typical current of 800 µA (at an output voltage of 5 V) through this resistance network, even without an external load.

13.3.7. Tracking output with an enable circuit

For the NEX91630-Q100 device, the EN pin functions together with ADJ pin, it cannot control separately via EN pin. Separating the enable function can be achieved using a circuit such as that referenced in Fig. 32.

When the input voltage at the EN/ADJ pin falls below the 0.7 V threshold, the NEX91630-Q100 is disabled and enters a sleep mode, drawing only 0.75 µA from the power supply. In typical applications, the reference voltage is often sourced from another regulator (such as a DC-DC converter or LDO voltage rail). This setup allows flexible enable/disable control via external I/O and circuitry, as shown in Fig. 32. In this example, the NEX90230-Q100, a 300 mA LDO with ultra-low quiescent current, serves as both the reference voltage source for the NEX91630-Q100 and as a power supply to the ADC.

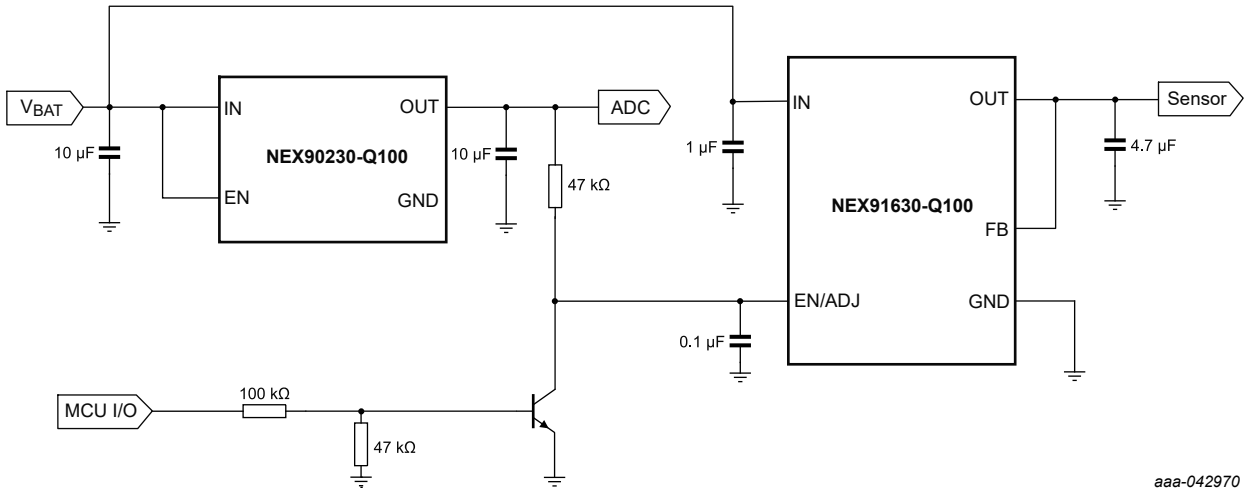


Fig. 32. Tracking an LDO with an enable circuit

13.3.8. Power-good (PG)

The power-good (PG) output signals an over-voltage or under-voltage condition on the tracking output by comparing the output voltage (V_{OUT}) against the external reference voltage (V_{ADJ}). When output voltage variations exceed the defined PG switching thresholds, this is indicated by a low-level signal at the PG output. Transient events shorter than the power-good reaction time (t_{PG_R}) will not activate the PG output. The PG deglitch time (t_{PG_D}) provides a start-up window for MCU or oscillators, representing the interval between threshold crossings and the PG output transitioning from low to high. This open-drain output requires the implementation of a pull-up resistor to a positive voltage rail.

Table 10 summarizes the PG response characteristics under various operating conditions.

Table 10. PG pin logic table

Device state		PG logic status	
		High impedance	Low impedance
Enable (EN = High)	V_{OUT} - V_{ADJ} < $V_{PG\ (UV)}$ V_{OUT} - V_{ADJ} > $V_{PG\ (OV)}$		√
Shutdown (EN = Low)			√
Thermal shutdown	T_j > T_{SD}	√	
$V_{IN(UVLO)}$	V_{IN} < 0.7 V	√	

13.4. Application implementation

13.4.1. Design requirements

A typical application is applied in automotive and power supply for an off-board sensor or multi sensor, which normally requires 5 V or 3.3 V output. The design parameters are specified in Table 11.

Table 11. Design parameters

Parameters	Value
Input voltage	4 V to 40 V
ADJ reference voltage	2 V to 20 V
Output voltage	2 V to 20 V
Output current	300 mA max
Output capacitor range	4.7 µF to 470 µF
Output capacitor ESR range	1 mΩ to 5 Ω

13.4.2. Typical application

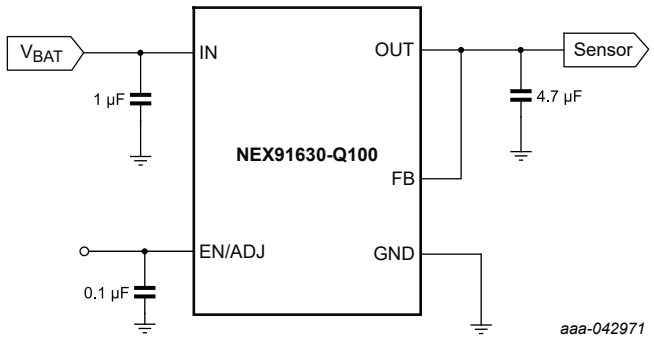


Fig. 33. NEX91630-Q100 typical application

13.4.2.1. Detailed design procedure

To begin the design process, determine the following requirements.

- Operation input voltage range
- Reference voltage
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor

13.4.2.1.1. Input capacitor

The NEX91x30-Q100 recommends an input decoupling capacitor connected from IN to GND and close to the IC terminals through is not required for stability, the value of which depends on the end-applications. The input supplies have a high impedance in some applications, thus placing the input capacitor on the input supply helps reduce the input impedance.

In addition, the input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. And several input capacitors can be placed in parallel to lower the impedance over frequency if the supply has a high impedance over a larger range of frequencies noise. The bigger-value input capacitors recommended when larger, fast rising time load/line transient are anticipated, or larger distance located from input power supply source. Lastly, the voltage rating of input capacitors must be greater than the maximum input voltage.

13.4.2.1.2. Output capacitor

To ensure the stability of the NEX91x30-Q100, the device requires:

- An output capacitor with a capacitance range of 4.7 µF to 470 µF (with a 30% derating applied under worst-case conditions) should be connected between the OUT and GND terminals.
- ESR range between 0.001 Ω and 5 Ω.

It is recommended to select X7R and X5R type ceramic capacitors with low ESR to improve the load transient response and ripple performance.

14. Layout

14.1. Layout guidelines

For best overall performance, it recommends the following guidelines for LDO layout:

- Place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections.
- Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface.
- The use of vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance.
- In most applications, the ground plane is necessary to meet thermal requirements.

A ground reference plane either embedded in the PCB itself or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad.

14.2. Layout examples

The figure below draws the layout example of NEX91630-Q100 device.

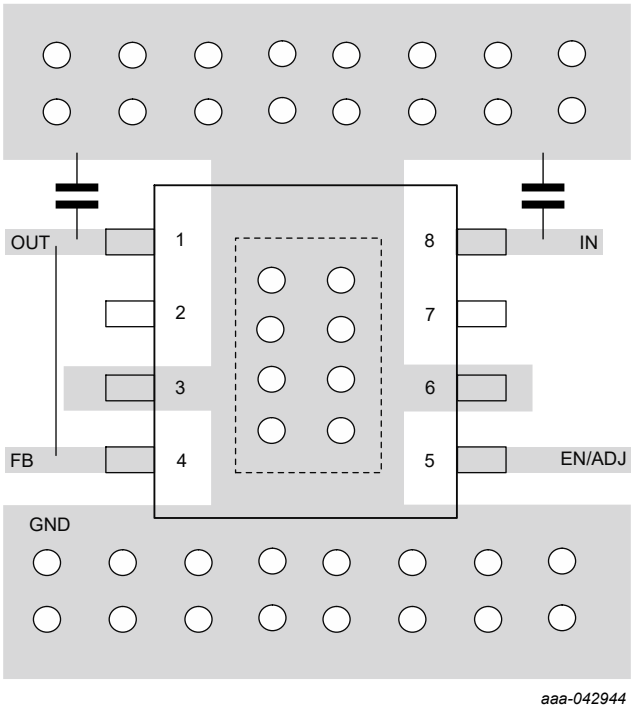
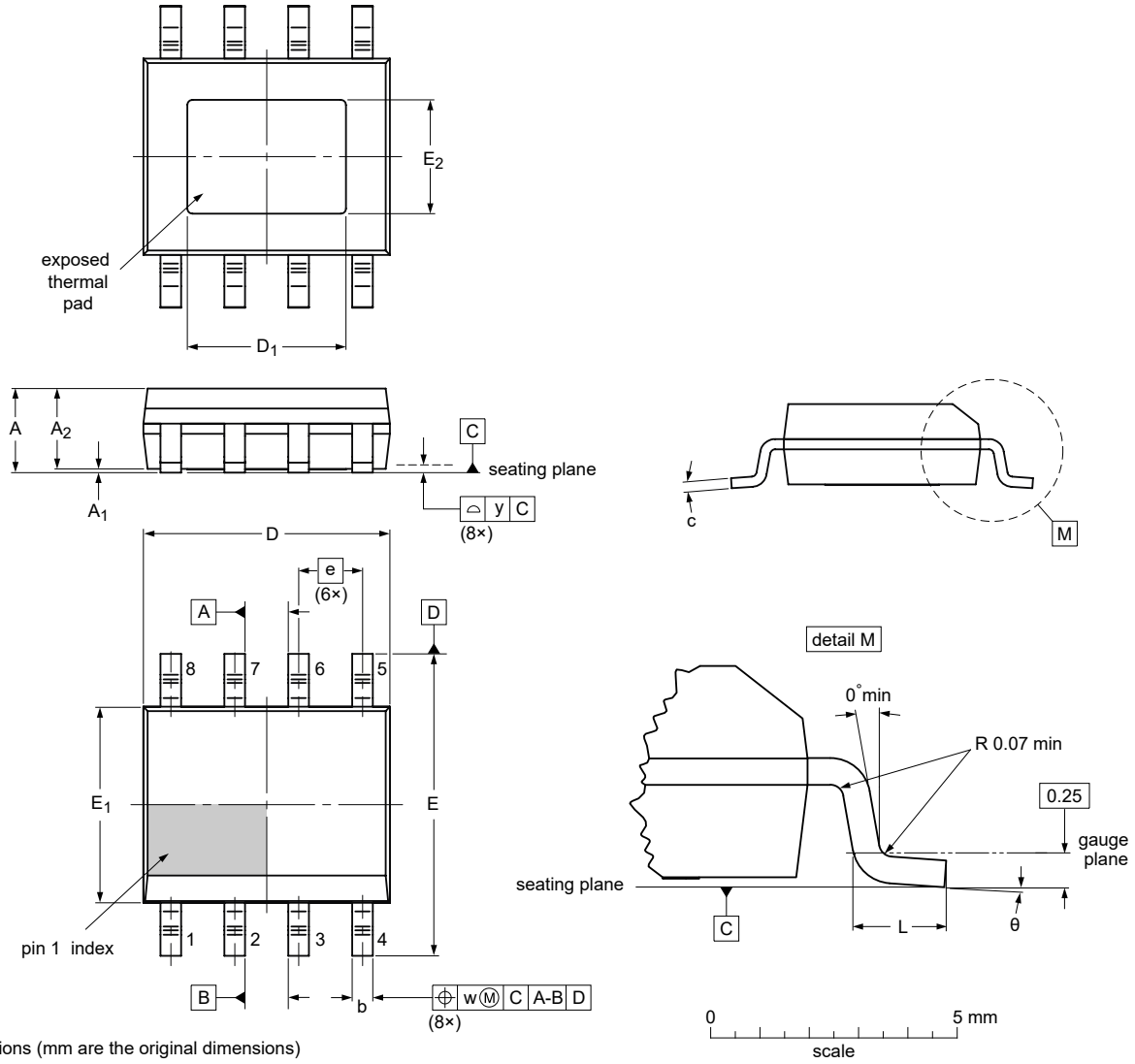


Fig. 34. NEX91630-Q100 layout example

15. Package outline

HSO8: Plastic, thermal enhanced small outline package; 8 leads; 1.27 mm pitch; 4.9 mm × 3.9 mm × 1.7 mm body **SOT8063-2**



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	b	c	D	D_1	E	E_1	E_2	e	L	y	w	θ
mm	max	1.70	0.10	1.55	0.51	0.25	5.00	3.25	6.20	4.00	2.36	1.27 BSC	1.27	0.10	0.25	8°
	nom															
	min	1.30	0.00	1.35	0.33	0.17	4.80	2.95	5.80	3.80	2.05		0.40			0°

Note
1. Dimension D and E_1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end or per side.
2. Dimension E_1 does not include interlead flash or protrusion.
3. Interlead flash or protrusion shall not exceed 0.25 mm per side.

sot8063-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8063-2		MS-012				~~25-04-09~~ 25-08-05

Fig. 35. Package outline SOT8063-2 (HSO8)

16. Abbreviations

Table 12. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
ANSI	American National Standards Institute
BCM	Body Control Module
CDM	Charged Device Model
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
ESR	Equivalent Series Resistance
HBM	Human Body Model
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
LDO	Low-DropOut
PCB	Printed Circuit Board
PG	Power-good
PMOS	P-channel Metal-Oxide-Semiconductor
PSRR	Power Supply Ripple Rejection
UVLO	Under-Voltage LockOut

17. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX91X30_Q100 v. 2.1	20250808	Product data sheet	-	NEX91X30_Q100 v. 2
Modifications:	• Fig. 35: Package outline updated.			
NEX91X30_Q100 v. 2	20250805	Product data sheet	-	NEX91X30_Q100 v. 1
Modifications:	• Overall update; NEX91730PB-Q100 information added.			
NEX91X30_Q100 v. 1	20250428	Product data sheet	-	-

18. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 8 August 2025